CLAIMS:

1. An electric or electronic circuit arrangement (100) comprising at least one, particularly layered carrier substrate (10) of a semiconducting or insulating material, at least one integrated circuit constituted by at least two spaced, particularly lithographically applied conductor tracks (20, 25) on the carrier substrate (10), at least one dielectric shielding layer (30; 35), particularly an insulation layer and/or passivation layer (30) and/or a further protective layer (35) situated between the conductor tracks (20, 25) and/or laterally with respect to the conductor tracks (20, 25) and/or on the conductor tracks (20, 25), provided for protecting the integrated circuit from external influences so that the integrated circuit has a specific, particularly lateral and/or particularly parasitic capacitance (C) determined by the dielectric shielding layer (30; 35), characterized in that at least one signal-generating unit (40), particularly at least an oscillator unit is connected to the contact terminals (22, 27) of the integrated circuit, the output frequency ($f_{meas.}$) of which unit is substantially determined by the specific capacitance (C), in that the signal-generating unit (40) precedes at least a first counting unit (50) which is clocked at the output frequency ($f_{meas.}$) of the signal-generating unit (40), in which counting unit an actual value count can be determined after a predetermined temporal counting period, in that at least a second counting unit (55) clocked at a reference frequency (f_{ref}) is provided, in which counting unit a nominal value count can be determined after the predetermined temporal counting period, in that the first counting unit (50) and the second counting unit (55) precede at least one comparator unit (60) for comparing the actual value count with the nominal value count, while the functions of the integrated circuit can be blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value count.

2. A circuit arrangement (100) as claimed in claim 1, characterized in that the conductor tracks (20, 25) are at least sectionally arranged parallel to each other and/or in a meandering intermeshing configuration.

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3. A circuit arrangement (100) as claimed in claim 1 or 2, characterized in that the mutual distance (d) between the conductor tracks (20, 25) is in the micrometer range.

4. A circuit arrangement (100) as claimed in any one of claims 1 to 3, characterized in that the material of the dielectric shielding layer (30; 35) is epoxy resin or silicon nitrite ($SiNO_2$) or silicon dioxide (SiO_2) or consists of other insulating layers used in the manufacture of semiconductors.

5. A circuit arrangement (100) as claimed in any one of claims 1 to 4, characterized in that the material of the dielectric shielding layer (30; 35) is also opaque.

6. A circuit arrangement (100) as claimed in any one of claims 1 to 5, characterized in that the signal-generating unit (40) comprises at least one oscillator circuit consisting of at least one capacitive unit, particularly a capacitor, and at least one resistive unit, particularly a resistor, and/or at least one oscillator circuit consisting of at least one capacitive unit, particularly a capacitor, and at least one inductive unit, particularly a coil.

7. A circuit arrangement (100) as claimed in any one of claims 1 to 6, characterized in that at least an evaluation unit (70), particularly at least a differential evaluation unit is constituted by the first counting unit (50), the second counting unit (55) and the comparator unit (60).

8. A circuit arrangement (100) as claimed in claim 7, characterized in that the evaluation unit (70) is implemented to detect a change of the specific capacitance (C) caused by an at least partial removal of the dielectric shielding layer (30; 35).

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9. A circuit arrangement (100) ad claimed in claim 7 or 8, characterized in that the evaluation unit (70) generates the error indication when the actual value deviates from the nominal range.

10. A circuit arrangement (100) as claimed in any one of claims 1 to 9, characterized in that the first counting unit (50) and/or the second counting unit (55) is formed on a digital basis.

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11. A card, particularly a chip card or smart card, ~~comprising at least an electric or electronic circuit~~ arrangement (100) as claimed in any one of claims 1 to 10.

12. A method of protecting an electric or electronic circuit arrangement (100) formed in accordance with the precharacterizing part of claim 1, from manipulation and/or abuse, characterized in that an output frequency ($f_{meas.}$) determined by the specific capacitance (C) is generated in at least one signal-generating unit (40), particularly in at least an oscillator unit, in that an actual value count is determined after a predetermined temporal counting period in at least a first counting unit (50) clocked at the output frequency ($f_{meas.}$) of the signal-generating unit (40), in that a nominal value count is determined after the predetermined temporal counting period in at least a second counting unit (55) clocked at a reference frequency (f_{ref}), in that the actual value count is compared with the nominal value count, and in that the functions of the integrated circuit are blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value count in at least one comparator unit (60).

13. A method as claimed in claim 12, characterized in that at least an evaluation unit (70) constituted by the first counting unit (50), the second counting unit (55) and the comparator unit (60) operates on a differential basis.

14. A method as claimed in claim 13, characterized in that a change of the specific capacitance (C) caused by an at least partial removal of the dielectric shielding layer (30; 35) is detected in the evaluation unit (70).

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15. A method as claimed in claim 13 or 14, characterized ~~in that the error~~ indication is generated in the evaluation ~~unit (70)~~ when the actual value deviates from the ~~nominal range~~.